

DOCKET NO: 295715US26PCT

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF :

MASARU SASAKI, ET AL.

: EXAMINER: MALEK, MALIHEH

SERIAL NO: 10/591,343 :

FILED: AUGUST 31, 2006

: GROUP ART UNIT: 2812

FOR: METHOD FOR MANUFACTURING :
SEMICONDUCTOR DEVICE AND
PLASMA OXIDATION METHOD

DECLARATION UNDER 37 C.F.R. §1.131

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

Now come:

Masaru Sasaki and Yoshiro Kabe who depose and state that:

1. We are named inventors in the above-identified application (i.e., U.S. 10/591,343).
2. We were employees of Tokyo Electron Limited of Tokyo, Japan at the time the present invention was conceived and reduced to practice and we are presently employees of Tokyo Electron Limited.
3. We are familiar with the prosecution history of the present application and/or counsel has explained to us the prosecution history of the present application.
4. Prior to November 22, 2002 we conceived and reduced to practice the invention described in the claims of the above-identified application.
5. The conception and reduction to practice of the presently claimed invention before July 28, 2003 is evidenced by the Extended Abstract of the 64th Autumn Meeting of the Japan

Society of Applied Physics August 30 - September 2, 2003 (i.e., the "Extended Abstract") which was published on the internet on June 8, 2003. An English translation of the Extended Abstract is attached as Appendix I.

6. The Extended Abstract describes a plasma processing method carried out using a mixed gas of oxygen and hydrogen on a stacked W/WN/Poly-Si layer. The method was conducted such that only the Poly-Si was oxidized. The W (i.e. Tungsten) was not oxidized. The disclosure of the Extended Abstract is reflected in paragraphs [0030]-[0032] of the present specification and claims (see for example pages 9 and 10).

7. The conception and reduction to practice of the presently claimed invention before November 22, 2002 is evidenced by an internal Tokyo Electron document titled "SPA Treatment for Post Date Oxidation" (i.e., the "Tokyo Electron document") which is attached as Appendix II. The date of the internal document has been redacted, however, the date is before November 22, 2002.

8. The Tokyo Electron document describes the conception and reduction to practice of the presently claimed invention before November 22, 2002. For example, page 2 of the Tokyo Electron document shows a semiconductor device formed from a film that is mainly W and a different film. A first layer of the film is oxidized by plasma processing.

9. The undersigned petitioner declares further that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under

Application No. 10/591,343

Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.

10. Further deponent saith not.

Masaru Sasaki
Masaru Sasaki

Apr. 17. 2009
Date

Yoshiro Kabe
Yoshiro Kabe

Apr. 17. 2009
Date

APPENDIX I

Extended Abstract of the 64th Autumn Meeting of the Japan Society of Applied Physics
August 30 - September 2, 2003 (English translation and original in Japanese)

CERTIFICATION

I, Junichi Aso, c/o Kanda Higashiyama BLDG., 2-1,
Kanda-tacyo, Chiyoda-ku, Tokyo, JAPAN hereby declare that I am
the translator of the following document and certify that the
translation is correct and accurate to the best of my knowledge and
belief:

Society of Applied Physics August 30-September 2,
2003 (i.e., the "Extended Abstract")

Signature of Translator: Junichi Aso

Dated: 28/04/2009

1p-A-5: Development of gate selective oxidation process by means
of SPA plasma

[Introduction]

With the miniaturizing of a transistor, it is required to reduce the resistance of a gate electrode of the transistor. In a DRAM or a FLASH memory, a WSi/poly-Si gate or a W/WN/poly-Si gate are utilized. The selective oxidation of gate etching is conducted by means of thermal oxidation process using a furnace or a RTO. However, since the thermal oxidation process is conducted at a higher temperature, the thermal oxidation process causes the fluctuation in V_{th} by the formation of birds beak and the contamination due to the sublimation of W. This presentation reports a selective oxidation process at low temperature using a SPA plasma of low electron temperature and high density.

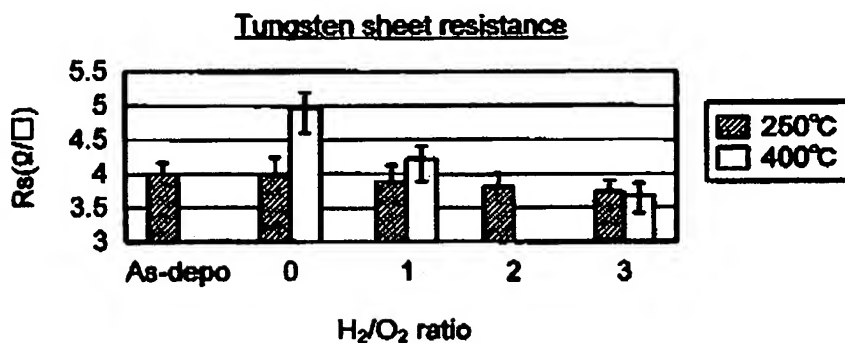
[Experiment]

Low temperature oxide plasma treatment is conducted for a gate electrode pattern of W/WN/poly-Si, and thus the configuration of the gate electrode pattern through the low temperature oxide plasma treatment by means of SEM and TEM. Moreover, sheet resistance measurement and XPS measurement are carried out for the W film. The XPS measurement is carried out for the surface and the depth of the W film.

[Result]

It was turned out that the abnormal oxidation of the W film was suppressed and oxide films were formed at the side walls of the poly-Si by the low temperature oxide plasma treatment through SEM and TEM. However, it was turned out that the oxidation of

the W film is proceeded by the low temperature oxide plasma treatment using oxide plasma through the resistance measurement and XPS analysis for the W film. In this point of view, the low temperature oxide plasma treatment using the plasma of the mixture of oxygen gas and hydrogen gas was conducted. In this case, the selective oxidation for the stacking structure was enhanced and the W film was not oxidized at all under the condition of $H_2/O_2=3$.



APPENDIX II

Tokyo Electron Document

(Document 3)

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Document 3

SPA Treatment for Post Gate Oxidation

Redacted

Tokyo Electron LTD.
Kansai Technology Center

KT#102-161



TOKYO ELECTRON

1

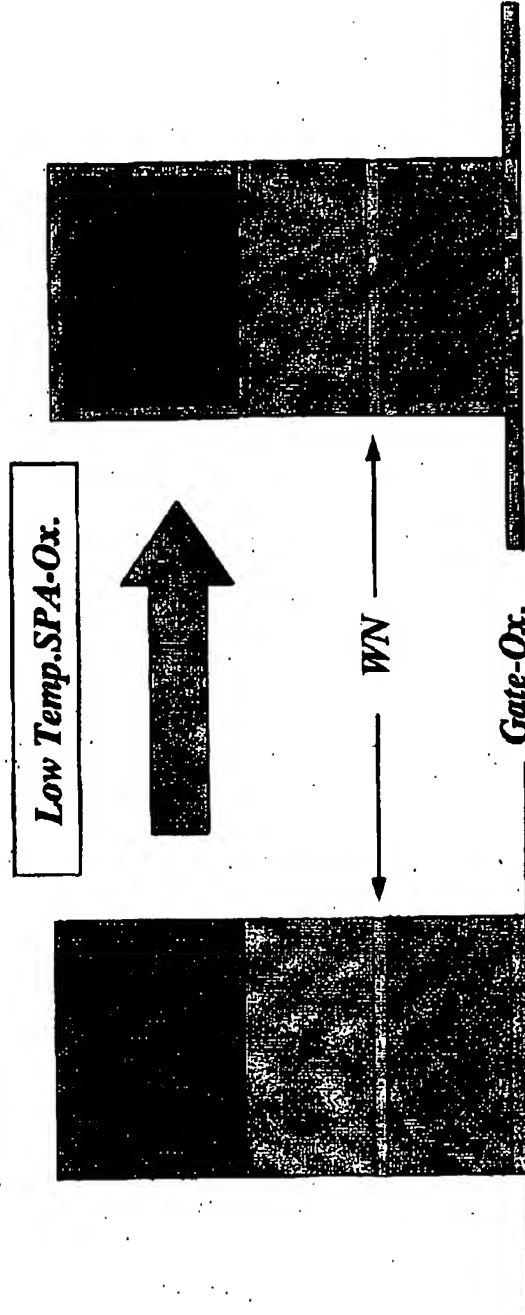
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Post Gate Oxidation

W-Poly metal



Advantage

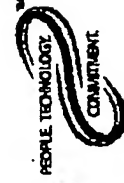
Low Temp. SPA-Ox. is a new process for post-gate oxidation.



TOKYO ELECTRON

2

Redacted



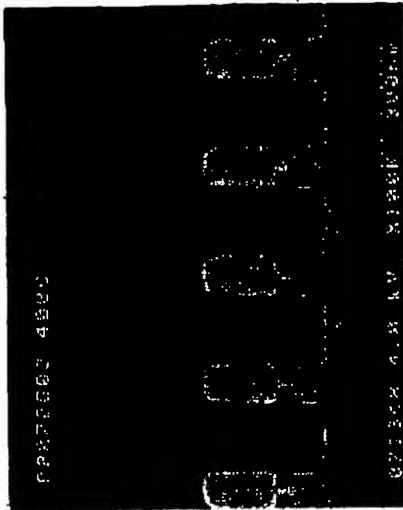
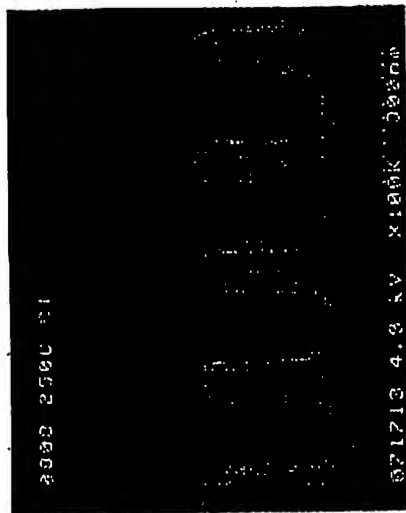
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Post Gate Oxidation

W-Poly metal

2.5nm on Si-Sub

3.5nm on Si-Sub



250°C 50sec.

400°C 110sec

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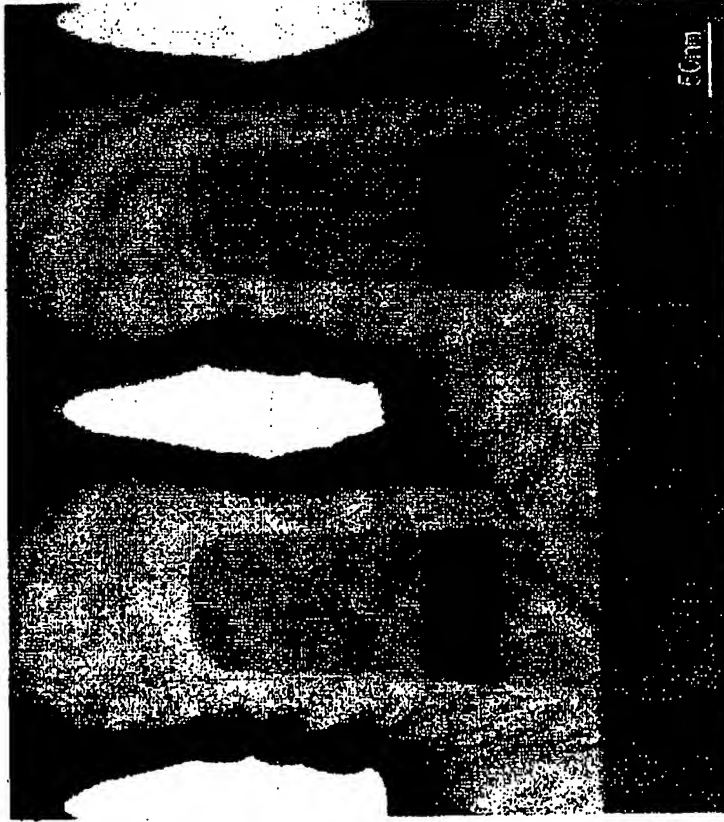
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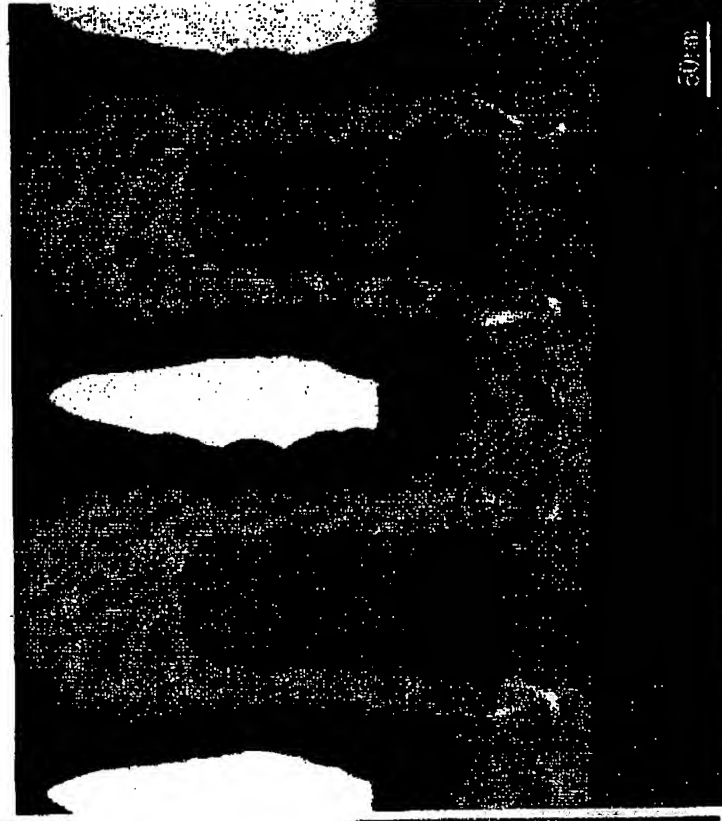
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Post Gate Oxidation

W-Poly Metal Gate



Reference (After Wet Clean)



Low Temp. SPA-Oxidation



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4

Rebated



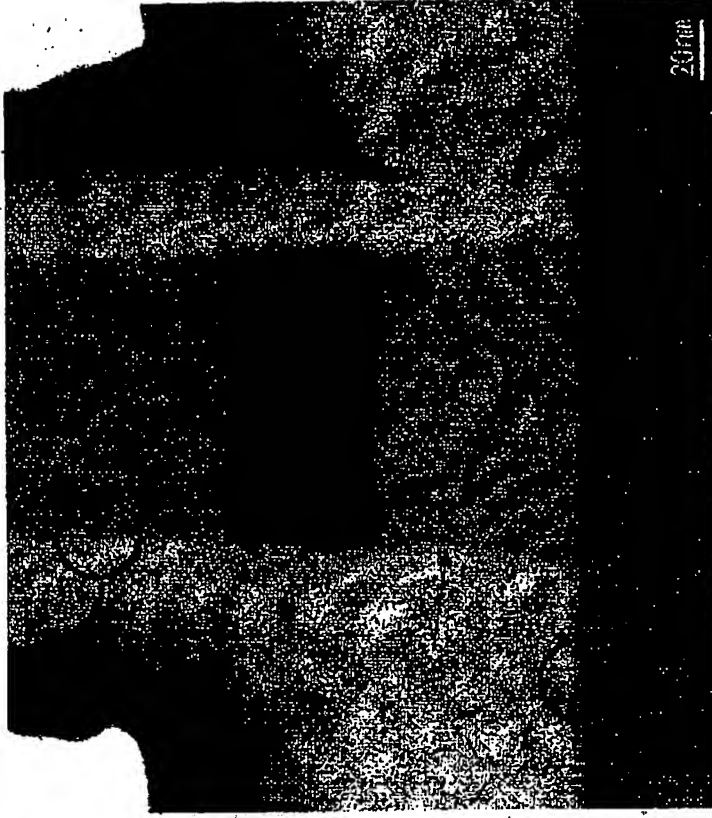
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Post Gate Oxidation

W-Poly Metal Gate



Reference (After Wet Clean)



Low Temp. SPA-Oxidation



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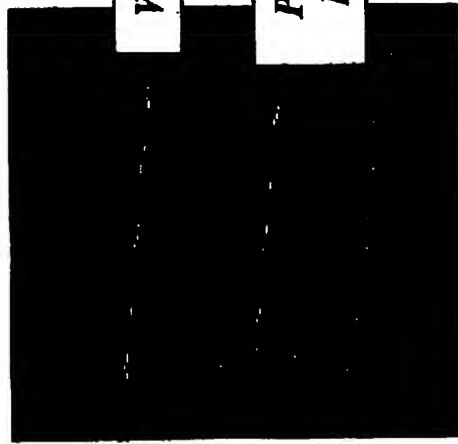
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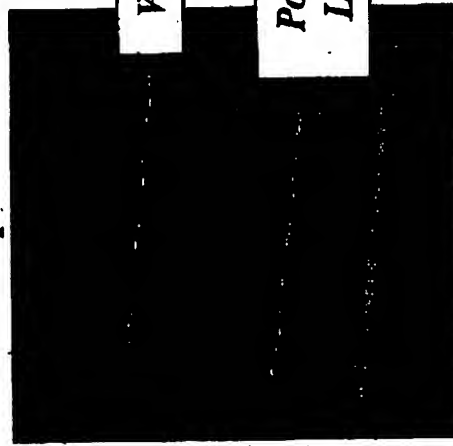
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EELS Line Profile (O)

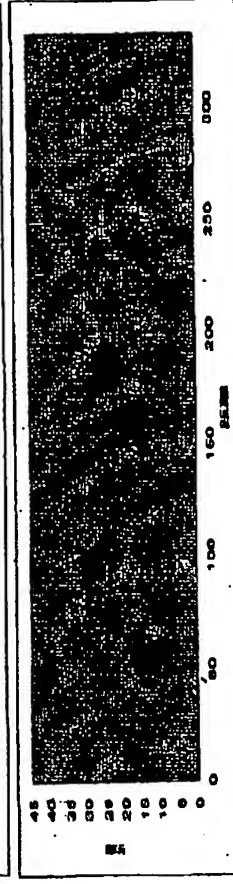
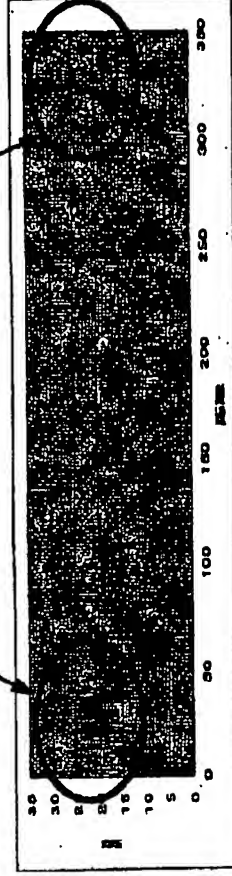
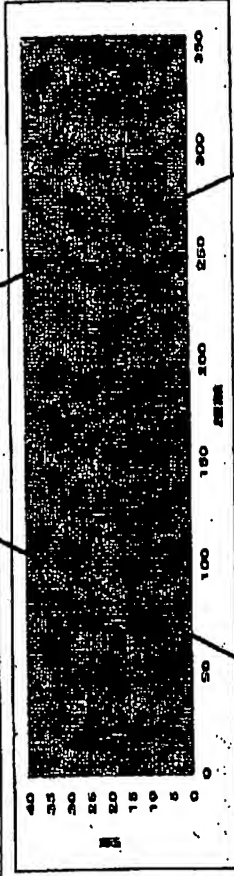
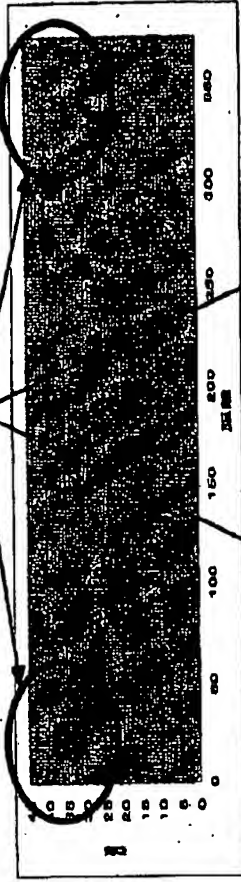
Reference



Low Temp. SPA-Ox.



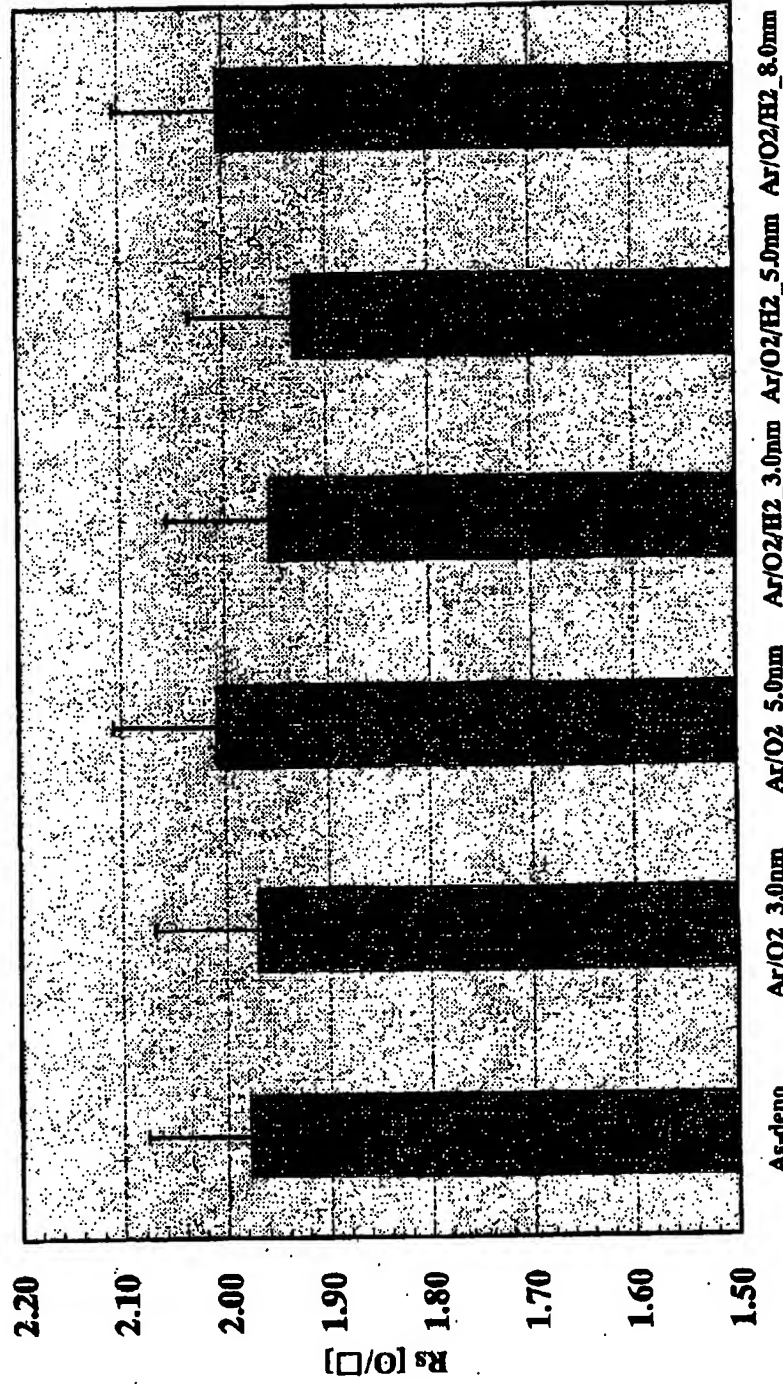
Same as Reference



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W film SPA-Ox. (Sheet Resistance)



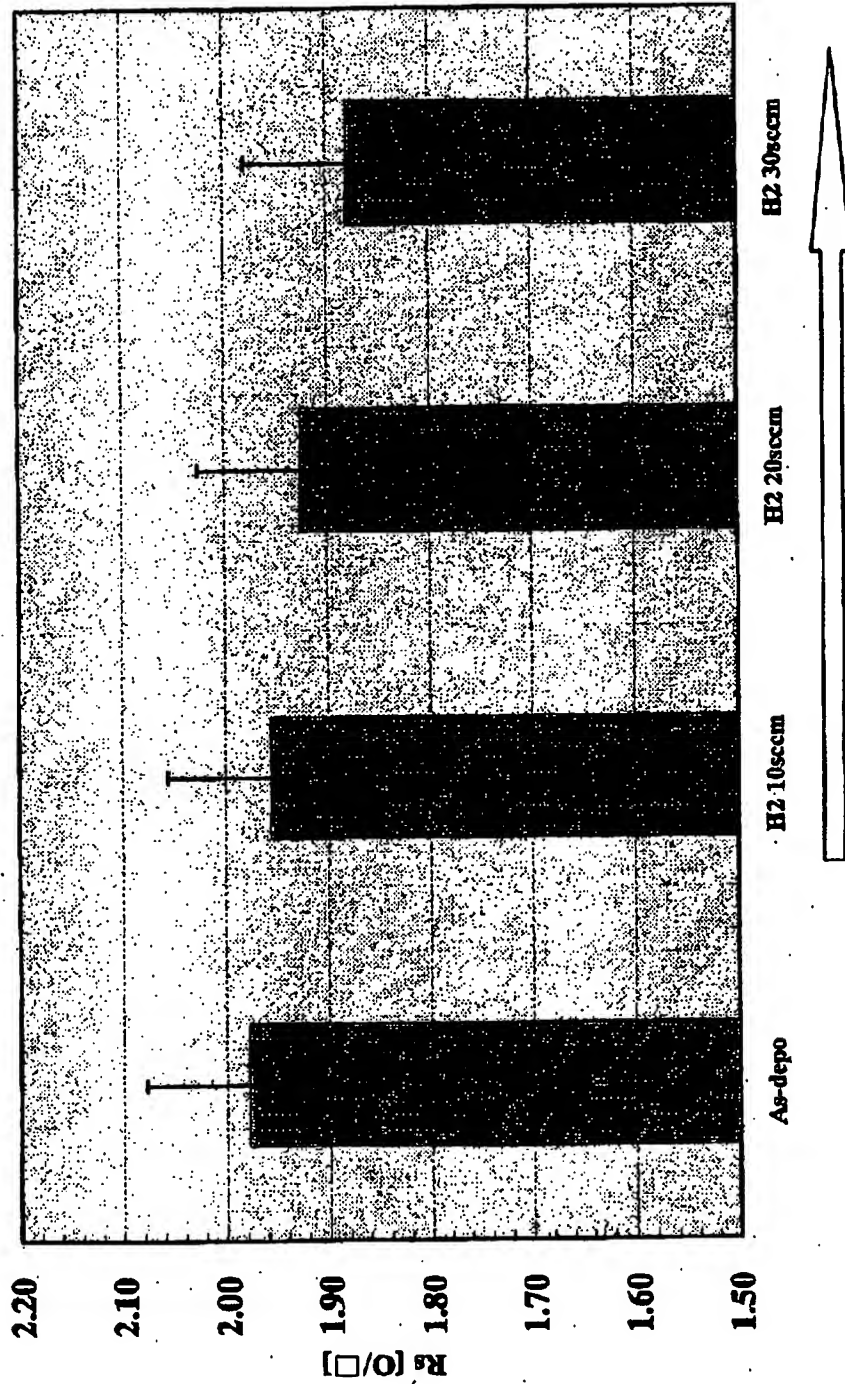
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W film SPA-Ox. (Sheet Resistance)



H₂ Flow Rate



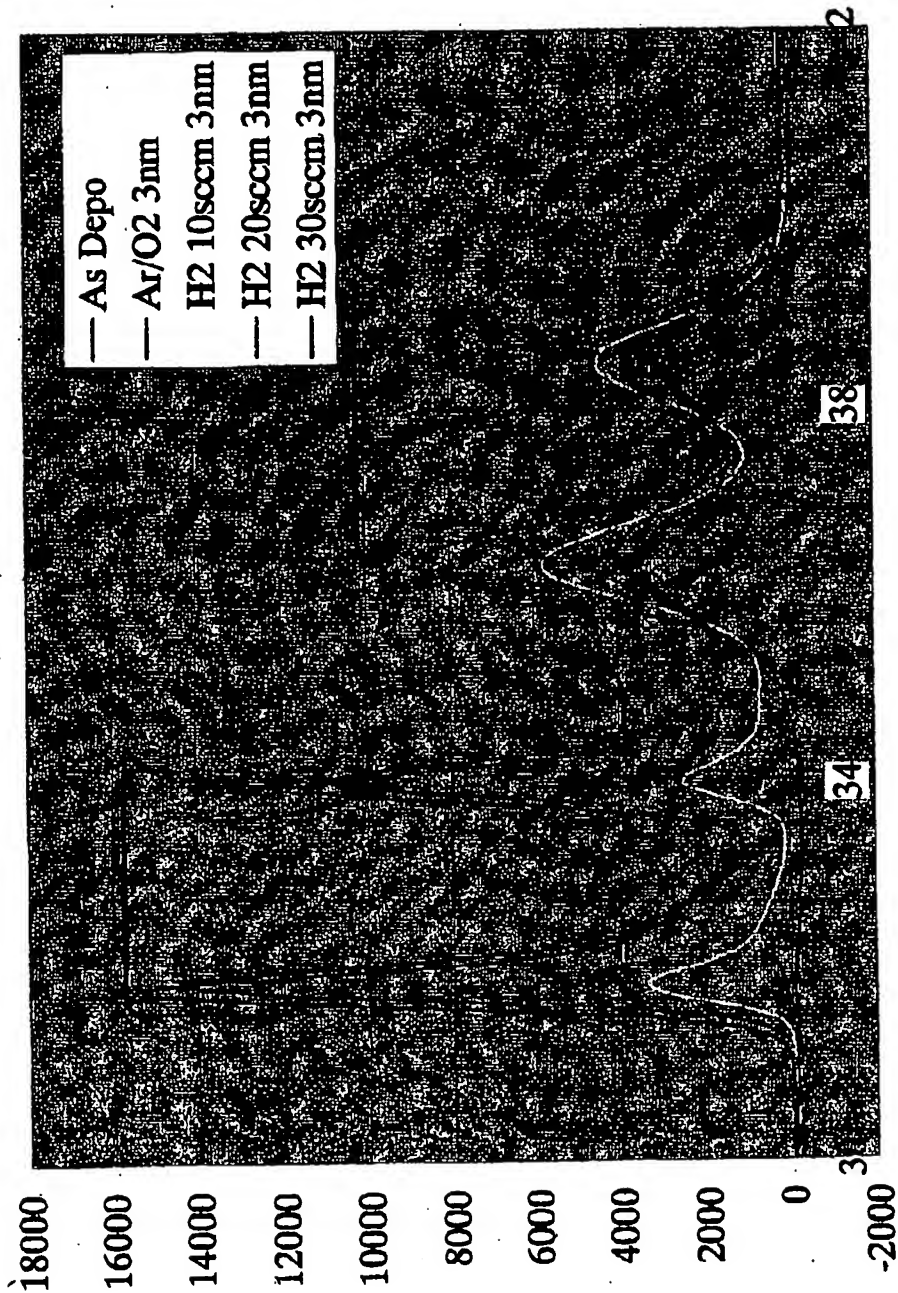
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XPS Analysis



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9

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